

Inventor: Gurtej S. Sandhu et al.

Title: Methods of Forming Transistors

Assignee: Micron Technology, Inc.

Docket No. MI22-1897

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

In compliance with 37 C.F.R. §§ 1.56, 1.97 and 1.98, your attention is directed to the United States patents and other references listed on the attached Form PTO/SB/08a. No admission is made regarding whether all the submitted references are prior art.

This Supplemental Information Disclosure Statement is being filed after the filing of the Request for Continued Examination (RCE) Application and before receipt of the first Office Action. Therefore, no fee is believed to be required. However, in the event that a fee is required for filing this Supplemental Information Disclosure Statement, please charge the fee specified under 37 C.F.R. §1.17(p) to Deposit Account No. 23-0925. Please credit Deposit Account No. 23-0925 with any overpayment of the above fee.

Citation of these references is respectfully requested.

Respectfully submitted,

Dated:

June 7, 2006

By:

Jennifer J. Taylor
Jennifer J. Taylor, Ph.D.
Reg. No. 48,711